**In The Claims:**

**Claims 1-2 (Cancelled)**

Claim 3. (Currently Amended) ~~The~~ A power-rail ESD protection circuit ~~of claim 2~~ with a dual trigger design, which is coupled between a first power line and a second power line connected to an IC device for protecting the IC device against ESD on the first power line and the second power line;

the power-rail ESD protection circuit comprising:

a control circuit, which is coupled between the first power line and the second power line, and which is capable of, in the event of ESD in the first power line and the second power line, being triggered by the ESD to output a substrate-triggering voltage and a gate-driving voltage; and

a NMOS device, whose source and drain are respectively connected to the first power line and the second power line, whose substrate is coupled to receive the substrate-triggering voltage, and whose gate is coupled to receive the gate-driving voltage, for bypassing ESD current from the first power line and the second power line,

wherein the control circuit includes $N$ serially-cascaded diodes, wherein the positive end of the first diode is connected to the first power line and the negative end of the last diode is connected to the second power line, and wherein the positive end of the ($A$)th diode is connected to the substrate of the NMOS device, and the positive end of the ($B$)th diode is connected to the gate of the NMOS device, where $A$ and $B$ are predetermined to allow the positive end of the ($A$)th

diode to supply the substrate-triggering voltage and the positive end of the (*B*)th diode to supply the gate-driving voltage; and wherein in the event of ESD in the first power line and the second power line, and the substrate-triggering voltage applied to the substrate of the NMOS device is greater than the gate-driving voltage applied to the gate of the NMOS device.

Claim 4. (Original) The power-rail ESD protection circuit of claim 3, wherein the *N* serially-cascaded diodes are implemented by *N* NMOS devices, each NMOS device having its drain and gate tied together and its source and substrate tied together.

**Claim 5. (Cancelled)**

Claim 6. (Currently Amended) ~~The~~ A power-rail ESD protection circuit ~~of claim 2~~ with a dual trigger design, which is coupled between a first power line and a second power line connected to an IC device for protecting the IC device against ESD on the first power line and the second power line;

the power-rail ESD protection circuit comprising:

a control circuit, which is coupled between the first power line and the second power line, and which is capable of, in the event of ESD in the first power line and the second power line, being triggered by the ESD to output a substrate-triggering voltage and a gate-driving voltage; and

a NMOS device, whose source and drain are respectively connected to the first power line and the second power line, whose substrate is coupled to receive the substrate-triggering voltage, and whose gate is coupled to receive the gate-driving voltage, for bypassing ESD current from the first power line and the second power line,

wherein the control circuit includes *N* serially-cascaded diodes, wherein the positive end of the first diode is connected to the first power line and the negative end of the last diode is connected to the second power line, and wherein the positive end of the (*A*)th diode is connected to the substrate of the NMOS device, and the positive end of the (*B*)th diode is connected to the gate of the NMOS device, where *A* and *B* are predetermined to allow the positive end of the (*A*)th diode to supply the substrate-triggering voltage and the positive end of the (*B*)th diode to supply the gate-driving voltage, and the substrate-triggering voltage applied to the substrate of the NMOS device is smaller than the gate-driving voltage applied to the gate of the NMOS device.

Claim 7. (Current Amended) The power-rail ESD protection circuit of claim 6, wherein the *N* serially-cascaded diodes are implemented by *N* NMOS devices, each NMOS device having its drain and gate tied together and its source and substrate tied together~~,~~ ~~T~~the *N* serially-cascaded diodes are implemented by *N* PMOS devices, each PMOS device having its drain and gate tied together and its source and substrate tied together.

**Claims 8-10 (Cancelled)**

Claim 11. (Currently Amended) A power-rail ESD protection circuit ~~of claim 8~~ with a dual trigger design, which is coupled between a first power line and a second power line connected to an IC device for protecting the IC device against ESD on the first power line and the second power line;

the power-rail ESD protection circuit comprising:

a control circuit, which is coupled between the first power line and the second power line, and which is capable of, in the event of ESD in the first power line and the second power line, being triggered by the ESD to output a substrate-triggering voltage and a gate-driving voltage; and

a PMOS device, whose source and drain are respectively connected to the first power line and the second power line, whose substrate is coupled to receive the substrate-triggering voltage, and whose gate is coupled to receive the gate-driving voltage, for bypassing ESD current from the first power line and the second power line,

wherein the control circuit includes *N* serially-cascaded diodes, wherein the positive end of the first diode is connected to the first power line and the negative end of the last diode is connected to the second power line, wherein the positive end of the (*A*)th diode is connected to the substrate of the PMOS device, and the positive end of the (*B*)th diode is connected to the gate of the PMOS, where *A* and *B* are predetermined to allow the positive end of the (*A*)th diode to supply the substrate-triggering voltage and the positive end of the (*B*)th diode to supply the gate-driving voltage; and wherein in the event of ESD in the first power line and the second power

line, and the substrate-triggering voltage applied to the substrate of the PMOS device is smaller than the gate-driving voltage applied to the gate of the PMOS device.

Claim 12. (Original) The power-rail ESD protection circuit of claim 11, wherein the *N* serially-cascaded diodes are implemented by *N* NMOS devices, each NMOS device having its drain and gate tied together and its source and substrate tied together.

**Claims 13-14 (Cancelled)**